

제 30회 한국반도체학술대회

The 30th Korean Conference on Semiconductors
2023년 2월 13일(월) - 15일(수) | 강원도 하이원리조트

대회명


제 30회 한국반도체학술대회

The 30th Korean Conference on Semiconductors (KCS 2023)

일시

2023년 2월 13일(월) - 15일(수)

장소

강원도 하이원 리조트 

규모

약 2,600명

주제

Semiconductor for a Sustainable Future

주관

 **SK 하이닉스**  **KSIA** 한국반도체산업협회  **COSAR** 한국반도체연구조합

주최

 **KPS** 한국물리학회 The Korean Physical Society  **MRS** 한국재료학회 Materials Research Society of Korea  **KIEE** 대한전기학회 The Institute of Electrical Engineers  **IEIE** 대한전자공학회 The Institute of Electronic and Information Engineers

 **IDEC** 반도체설계교육센터 IC DESIGN EDUCATION CENTER  **ISE** 반도체공학회 The Institute of Semiconductor Engineers  **KSSD** 한국반도체디스플레이기술학회 The Korean Society of Semiconductor & Display Technology

후원

 **GWTO** 강원도관광재단 Gangwon Tourism Organization  **SK 하이닉스**  **SAMSUNG**  **DB하이텍**

 **Silicon Mitus**  **JUSUNG ENGINEERING**  **ASML**  **DONGJIN SEMICHEM CO., LTD.**  **AURUS Technology**

 **WONIK IPS**  **Lam RESEARCH**  **KLA+**  **Uni Test**  **APPLIED MATERIALS**

 **TEL**  **DONGWOO FINE-CHEM**  **SYNOPTIS** Silicon to Software  **TU TechwidU** Technology with you  **Adaptive Plasma**

 **NEXTIN**  **FST FINE SEMITECH CORP.**  **MiCo Family** MiCo, MiCo Ceramics, KoMiCo  **soubrain**  **Lot vacuum** Leader in Technology Vacuum

 **HANA MICRON**  **PSK**  **Telechips**  **ZEISS**  **semi cadence**

프로그램

- 기조강연
- 초대강연
- Short Course
- Rump Session
- 구두세션
- 포스터세션
- 기업체 전시
- 강대원상 시상식
- 만찬
- Chip Design Contest

문의

제 30회 한국반도체학술대회 사무국

전화 042-472-7460 | 팩스 +82-42-472-7459 | 이메일 kcs@ksia.or.kr



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The 30th Korean Conference on Semiconductors

2023년 2월 13일(월)~ 15일(수) | 강원도 하이원리조트(그랜드호텔 컨벤션타워)

2023년 2월 15일(수), 10:45-12:30

Room E (루비 II, 5층)

E. Compound Semiconductors 분과 [WE2-E] Compound Semiconductor II

좌장: 차호영 교수(홍익대학교)

<p>WE2-E-1 10:45-11:15 [초청]</p>	<p>Near-Junction Thermal Management for High-Power Electronics Jungwan Cho <i>School of Mechanical Engineering, Sungkyunkwan University</i></p>
<p>WE2-E-2 11:15-11:30</p>	<p>Impact of $\text{Hf}_x\text{Al}_{1-x}\text{O}$ Gate Dielectric in the Performance Enhancement of AlGaN/GaN High Electron Mobility Transistors Ju-Won Shin¹, Walid Amir¹, Surajit Chakraborty¹, Atish Bhattacharjee¹, Hyo-Joung Kim¹, Jae-Moo Kim², and Tae-Woo Kim¹ ¹<i>School of Electrical, Electronic, and Computer Engineering, University of Ulsan</i>, ²<i>KANC</i></p>
<p>WE2-E-3 11:30-11:45</p>	<p>Cryogenic Switches based on InGaAs HEMT for Quantum Signal Routing Jaeyong Jeong¹, Seong Kwang Kim¹, Jongmin Kim², Jisung Lee³, Joon Pyo Kim¹, Bong Ho Kim¹, Yoon-Je Suh¹, Dae-Myeong Geum¹, Seung-Young Park³, and SangHyeon Kim¹ ¹<i>School of Electrical Engineering, KAIST</i>, ²<i>KANC</i>, ³<i>KBSI</i></p>
<p>WE2-E-4 11:45-12:00</p>	<p>In_{0.53}Ga_{0.47}As MOS Interface Optimization Using Post Deposition Annealing and Post Metal Annealing for Photo-FET on Si Wafer Sung-Han Jeon^{1,2}, Dae-Hwan Ahn¹, Jindong Song¹, Woo-Young Choi², and Jae-Hoon Han¹ ¹<i>Center for Opto-Electronic Materials and Devices, KIST</i>, ²<i>Department of Electrical and Electronic Engineering, Yonsei University</i></p>
<p>WE2-E-5 12:00-12:15</p>	<p>Positive-Bias-Stress Instability Assessment of AlGaN/GaN HEMTs during On-State Condition Walid Amir¹, Ju-Won Shin¹, Ki-Yong Shin¹, Surajit Chakraborty¹, Takuya Hoshi², Takuya Tsutsumi², Hiroki Sugiyama², Hideaki Matsuzaki², and Tae-Woo Kim¹ ¹<i>Department of Electrical, Electronic, and Computer Engineering, University of Ulsan</i>, ²<i>NTT Device Technology Laboratories, NTT Corporation</i></p>
<p>WE2-E-6 12:15-12:30</p>	<p>Study of Delta-doping Dopants on GaAs Tunnel Junctions and Their Thermal Degradation toward High Efficiency III-V/Si Tandem Cell May Angelu Madarang^{1,2}, Rafael Jumar Chu^{1,2}, Yeonhwa Kim^{1,3}, Eunkyo Ju¹, Quang Nhat Dang Lung^{1,2}, Tae Soo Kim^{1,4}, Won Jun Choi¹, and Daehwan Jung^{1,2} ¹<i>Center for Opto-Electronic Materials and Devices, KIST</i>, ²<i>Division of Nano and Information Technology, University of Science and Technology (UST)</i>, ³<i>Department of Materials Science and Engineering, Korea University</i>, ⁴<i>School of Electrical and Electronic Engineering, Yonsei University</i></p>

In_{0.53}Ga_{0.47}As MOS Interface Optimization Using Post Deposition Annealing and Post Metal Annealing for Photo-FET on Si Wafer

Sung-Han Jeon^{1,2}, Dae-Hwan Ahn¹, Jindong Song¹, Woo-Young Choi², Jae-Hoon Han^{1*}

¹Center for Opto-Electronic Materials and Devices, Korea Institute of Science and Technology (KIST),
²Department of Electrical and Electronic Engineering, Yonsei University, Korea

SWIR (Short-wave infrared) detectors are widely used in Si Photonics, medical devices, LiDAR sensors, and quantum computing. Especially, In_{0.53}Ga_{0.47}As has been used to detect SWIR wavelengths due to lattice-matched InP wafer and high absorption coefficient. The PIN and APD structures are widely used in the In_{0.53}Ga_{0.47}As photodetector. However, there are challenges in the detection of weak light since PIN does not provide any internal gain and APD suffers from the high operating voltage with a large excess noise [1]. To solve the aforementioned problems, Photo-FETs, which have middle internal gain and low operating voltage, have been researched. Recently, organic and 2D material-based Photo-FET structures have been widely studied, but these materials are unsuitable for the SWIR region due to low mobility [2].

In our previous research, In_{0.53}Ga_{0.47}As based Photo-FET were fabricated by using wafer bonding technology, and optical properties with various device channel lengths were investigated. However, a decrease of I_{ph} was observed at the saturation voltage region. We have assumed that the In_{0.53}Ga_{0.47}As interface and oxide trap led to a decrease of I_{ph}.

In this study, to optimize the optical properties of the Photo-FET, the In_{0.53}Ga_{0.47}As MOS capacitor was fabricated and C-V curves are measured to evaluate the D_{it} and slow trap density. Figure 1 shows In_{0.53}Ga_{0.47}As Photo-FET structure and cross-section. Figure 2 shows the C-V curves with post-deposition annealing (PDA) and post-metal annealing (PMA) conditions at 350 °C for 10min. Figure 3 shows D_{it} at PDA and PMA in 350 °C conditions calculated with the Terman method. This research proposes MOS interface condition optimized D_{it} and slow trap to evaluate the optical property of In_{0.53}Ga_{0.47}As Photo-FET.

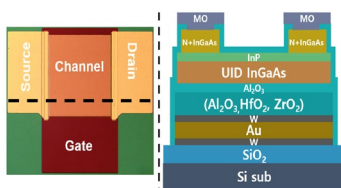


Fig. 1 Photo-FET structure and cross-section

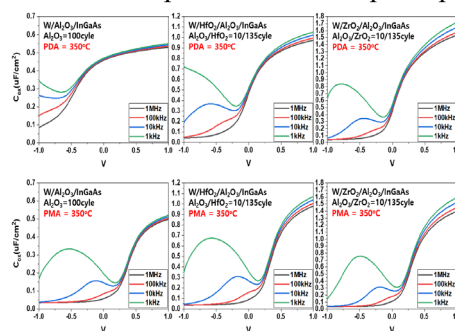


Fig. 2 W/high-k/Al₂O₃/In_{0.53}Ga_{0.47}As MOS capacitor with PMA and PDA C-V curve

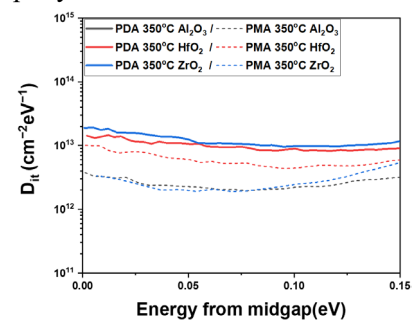


Fig. 3 D_{it} of W/high-k/Al₂O₃/In_{0.53}Ga_{0.47}As MOS capacitor

Acknowledgments This work was supported in part by the Institutional Program (2E31532) funded by KIST, and in part by the NRF (Grant No. NRF-2022M3F3A2A01085469 and NRF-2022R1C1C1007333), and the Institute of Information & Communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (No. 2022-0-00208).

References [1] J.J.S. Huang et al., "Temperature dependence study of mesa-type InGaAs/InAlAs avalanche photodiode characteristics," *Advances in Optoelectronics* 2017. [2] F. H. L. Koppens et al., "Photodetectors based on graphene, other two-dimensional materials and hybrid systems," *Nat. Nanotechnol* 2014.